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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/901,936	NOONBURG, DEREK B.	
	Examiner	Art Unit	
	Joni Hsu	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 24, 2007 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claims 1-41 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's arguments, see pages 13, 16-17, filed April 24, 2007, with respect to the rejection(s) of claim(s) 1-6, 14-17, 19-32, and 34-41 under 35 U.S.C. 102(b) and 7-13, 18, and 33 under 35 U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Rege (US005390299A).

4. With regard to Claims 1-20 and 23-41, Applicant argues that Artieri (US005579052A) does not teach that at least one data packet contains data fetched from each of a plurality of memory pages (pages 13, 16-17).

In reply, the Examiner agrees. However, new grounds of rejection are made in view of Rege.

5. With regard to Claims 21-22, Applicant argues that Artieri does not teach determining a packetization scheme used to packetize the data into data packets based upon the locations in memory of the data (page 17).

In reply, the Examiner has made a new grounds of rejection in view of Rege, which more clearly teaches this limitation.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 14, 15, 19, and 24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Rege (US005390299A).

8. With regard to Claim 1, Rege discloses a method for generating memory requests to fetch read data from a plurality of locations in a memory (200, Figure 2; *in response to the PMC RX DONE signal, the host bus interface then reads the packet data from the packet buffer memory 200*, Col. 7, lines 36-39), the memory comprising a plurality of

memory pages (305, Figure 3; *packet buffer memory 200 containing a pool of pages 300, pool of pages 300 is an array of pages 305*, Col. 6, lines 14-18) each of the memory pages having a plurality of words (*converts the serial packet data into parallel data words, page of data*, Col. 6, lines 60-65), the method comprising the steps of determining the locations of the read data in the memory (*each ring entry 306 contains a "pointer" 310, pointer 310 is the staring address of one page 305 that contains packet data, memory controller 203 can read the ring entry 306*, Col. 6, lines 29-35, 57-59). Packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (Col. 6, lines 18-22). Therefore the packetization scheme is selected based on how many pages of data need to be read. Since the memory stores the plurality of pages (Col. 6, lines 14-18), this means that each page has a location in the memory. Therefore, the packetization scheme is selected based on the locations of the read data (Col. 6, lines 18-22). Rege discloses assembling at least one read command for addressing the plurality of locations of the read data; and fetching the read data from the memory locations and combining it into a plurality of data packets in accordance with the selected packetization scheme, wherein at least one data packet contains data from more than one of the plurality of memory pages (*packet buffer memory 200 containing a pool of pages 300, packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc., each ring entry 306 contains a "pointer" 301,a length field 312, pointer 310 is the starting address of one page 305 that contains packet data, length field 312 indicates the length of the packet in bytes*, Col. 6, lines 12-48, 60-68; *host bus interface 201 then reads the packet data from the packet buffer memory 200*, Col. 7, lines 1-12, 36-48).

9. With regard to Claim 2, Rege discloses the step of sending the at least one read command corresponding to the plurality of data packets to the memory (*when the node 100 is transmitting, the CPU 101 informs the adapter 103 that there is a packet of data in memory 102 to be transmitted on the network bus 105, the adapter 103 reads the packet from memory 102 and transmits it over the network bus 105*, Col. 4, lines 59-65; *CPU 101 passes commands to the adapter 103*, Col. 5, lines 31-39).

10. With regard to Claim 3, Rege discloses the step of fetching the read data in response to sending the at least one read command (Col. 4, lines 59-65; Col. 5, lines 31-39).

11. With regard to Claim 14, Rege discloses that each of the at least one read command includes specifications for combining selected ones of the plurality of words from selected ones of the plurality of memory pages into the plurality of data packets (*packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc., length field 312 indicates the length of the packet in bytes, when a packet is received from the network, the network interface 202 converts the serial packet data into parallel data words, and stores the words in the packet buffer memory 200*, Col. 6, lines 18-22, 40-48, 60-63; *reads the packet data from the packet buffer memory 200*, Col. 7, lines 36-39; Col. 4, lines 59-65; Col. 5, lines 31-39).

12. With regard to Claim 15, Rege discloses that if there are not enough pages available for subsequent packets, then subsequent packets are discarded (Col. 10, lines 18-23), which means that the plurality of packets cannot exceed a predetermined number. Therefore, the plurality of data packets is equal to or less than a predetermined number.

13. With regard to Claim 19, Rege discloses a method for packing read data into data packets (Col. 6, lines 18-22), the read data being stored in a plurality of locations in a memory (200, Figure 2; Col. 7, lines 36-39), the memory comprising a plurality of memory pages (305, Figure 3; Col. 6, lines 14-18). Packets are transmitted from one node 100 to another (Col. 4, lines 57-59). Each node 100 comprises a CPU 101, host memory 102, and network adapter 103 (Col. 4, lines 44-46). The adapter 103 stores the packets in host memory 102 by first storing the packet data in a packet buffer memory 200 (Col. 5, lines 40-45; Col. 6, lines 12-22), then reading the packet data from the packet buffer memory 200 and writing it into the host memory 102 (Col. 7, lines 36-39). Packets are transmitted by the adapter 103 reading the packet from memory 102 and transmitting it over the network bus 105. Within the packet is the address of the destination node on the network (Col. 4, lines 59-66). The CPU 101 accesses the adapter control and status registers to control and monitor the operation of the adapter 103 (Col. 5, lines 15-20), and the CPU 101 can pass commands to the adapter 103 (Col. 5, lines 29-39). Therefore, the CPU 101 sends read commands to the adapter 103, and in response to the read commands (Col. 5, lines 15-20, 29-39), the adapter reads data from memory 102 and transmits it over the network bus 104 to the destination node on the network (Col. 4, lines 59-66). The destination node receives the packet through its adapter 103 (Col. 4,

line 67-Col. 5, line 12). The adapter 103 receives the packets (Col. 5, lines 1-4, 40-45) and stores the packets in the packet buffer memory 200 containing a pool of pages 300. The pool of pages 300 is an array of pages 305, which are 512 bytes large, so that packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (Col. 6, lines 13-22). Therefore, the adapter 103 receives data read from the memory 102 of the source node (Col. 4. line 67-Col. 5, line 12) and packs the read data received into the data packets that are stored in the packet buffer memory 200 of the destination node (Col. 5, lines 40-45; Col. 6, lines 13-22). Since the CPU 101 sends commands to the adapter 103 to control the adapter 103 (Col. 5, lines 14-20, 29-39), the CPU 101 sends commands to the adapter 103 including specifications on reading data from the packet buffer memory 200 of the source node (Col. 7, lines 36-39; Col. 4, lines 49-66) and how the data is to be packed into data packets that are stored in the packet buffer memory 200 of the destination node (Col. 4, lines 49-68; Col. 5, lines 1-12, 14-20, 29-45; Col. 6, lines 13-22). Therefore, the method comprises the steps of receiving at least one read command requesting the read data, the at least one read command comprising specifications for including in the data packets a plurality of selected portions of the read data from the plurality of memory pages; sending instructions to the memory (memory 102 of the source node 100) according to the at least one read command received, the instructions relating to a manner in which the read data requested is to be obtained from the memory (Col. 4, lines 44-46, 49-66; Col. 5, lines 40-45; Col. 6, lines 12-22; Col. 7, lines 36-39); receiving the read data from the memory in response to the memory receiving the instructions; and packing the read data received into the data packets according to the specifications of each of the at least one

read commands, wherein at least one data packet contains data form more than one of the plurality of memory pages (Col. 4, lines 49-68; Col. 5, lines 1-12, 14-20, 29-45; Col. 6, lines 13-22).

14. With regard to Claims 24 and 26, Claims 24 and 26 are similar in scope to Claim 1, and therefore is rejected under the same rationale.

15. With regard to Claims 25 and 27, Claims 25 and 27 are similar in scope to Claim 19, and therefore is rejected under the same rationale.

16. Thus, it reasonably appears that Rege describes or discloses every element of Claims 1-3, 14, 15, 19, and 24-27 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A).

20. With regard to Claim 16, Rege discloses that the selected ones of the plurality of memory pages is two (Col. 6, lines 18-22). Rege discloses a predetermined threshold of pages, and detecting overflow when a packet is discarded due to lack of free pages (Col. 2, lines 10-15). Rege does not explicitly teach that the predetermined number is four. However, it would be obvious to adjust the predetermined threshold of pages to any number, and therefore the predetermined number of packets can be any number, and therefore can be four.

why? (motivation)

21. With regard to Claim 17, Rege discloses packets between 512 and 1024 bytes are stored in two pages 305, etc., meaning that if the size of the packets is bigger, they can be stored in three pages. Rege discloses a predetermined threshold of pages, and detecting overflow when a packet is discarded due to lack of free pages (Col. 2, lines 10-15). Rege does not explicitly teach that the predetermined number is four. However, it would be

obvious to adjust the predetermined threshold of pages to any number, and therefore the predetermined number of packets can be any number, and therefore can be four. motivation?

22. Claims 4, 10, 11, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A) in view of McGuinness (US006104416A).

23. With regard to Claim 4, Rege is relied upon for the teachings as discussed above relative to Claim 1.

However, Rege does not specify what type of data is being read, and does not teach that the read data comprises a reference pixel chunk having a luminance chunk and a chrominance chunk. However, McGuinness discloses that the read data comprises a reference pixel chunk having a luminance chunk and a chrominance chunk (*luminance and chrominance components of each picture are stored, pixels in picture blocks, reference pictures*, Col. 4, lines 40-52). The luminance chunks and chrominance chunks are stored in memory (Col. 4, lines 40-52). An arbitrary array portion of the digital array is retrieved from the memory. The word address corresponding to the first datum of the array portion is determined. The number of tiles that contain data in the array portion is determined. The desired array portion is then read from memory by reading a part of each tile in one memory burst (Col. 3, lines 36-42). Therefore, the addresses of the luminance chunk and chrominance chunk data to be read in one memory burst are determined, and the data is read from those addresses in one memory burst. Therefore, the data to be read in one memory burst is selected based on the location of the luminance chunk and chrominance chunk. Since Rege teaches selecting packetization scheme based

on location of the data, the method of Rege can be modified so that the data comprises luminance chunks and chrominance chunks, and the data to be read in one memory burst for a packet is selected based on the location of the luminance chunk and the chrominance chunk, as suggested by McGuinness, and selecting the data to be read for a packet is considered to be selecting the packetization scheme.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify Rege's method of selecting a packetization scheme so that it is used for reading data comprising a reference pixel chunk having a luminance chunk and a chrominance chunk as suggested by McGuinness because McGuinness suggests that transmitting an encoded bitstream for video is needed in many applications, such as watching television or using a DVD player or a computer (Col. 1, lines 48-53, 63-67; Col. 2, line 1). An encoded bitstream for video includes a reference pixel chunk having a luminance chunk and a chrominance chunk (Col. 4, lines 33-52). Therefore, it would be advantageous to implement Rege's efficient method of transferring data by selecting a packetization scheme (Col. 1, lines 10-13; Col. 6, lines 18-22, 60-68; Col. 7, lines 1-12, 36-48 in Rege) so that it is used for reading data comprising a reference pixel chunk having a luminance chunk and a chrominance chunk as suggested by McGuinness.

24. With regard to Claim 10, Rege does not teach the step of placing a virtual memory page boundary across the luminance chunk, the virtual memory page boundary being associated with the packetization scheme. According to the disclosure of this application, a virtual page boundary is placed to split the left 2 words of each row. Therefore, the chunk is still considered as falling across four pages A-D. However, pages

B and D are actually part of pages A and C [0069-0070]. This is done to create a symmetry that allows the reduction of the number of cases that need to be considered for packetization [0068]. McGuinness describes interlacing the luminance Y and both chrominance Cr and Cb so that all of the components can be retrieved in one word, reducing latency during rasterization without increasing the time needed to retrieve pixels for decoding because all of the components for one tile can still be retrieved in one burst (Col. 10, lines 26-30). Storing the chrominance components so interlaced enables the FIFO that stores the chrominance to have the same structure as the FIFO storing the luminance (Col. 10, lines 8-9), and therefore creates symmetry. Therefore, McGuinness discloses the step of placing a virtual memory page boundary across the luminance chunk, the virtual memory page boundary being associated with the packetization scheme.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Rege to include the step of placing a virtual memory page boundary across the luminance chunk, the virtual memory page boundary being associated with the packetization scheme as suggested by McGuinness because McGuinness suggests the advantage of reducing latency for reading an encoded bitstream for video (Col. 9, line 60-Col. 10, line 9; Col. 2, lines 8-18). It would have been obvious to modify Rege's method of selecting a packetization scheme so that it is used for reading an encoded bitstream for video for the same reasons given in the rejection for Claim 4.

25. With regard to Claim 11, Rege does not teach the step of placing a virtual memory page boundary across the chrominance chunk, the virtual memory page boundary being associated with the packetization scheme. According to the disclosure of this application, a virtual page boundary is placed to split the left 2 words of each row. Therefore, the chunk is still considered as falling across four pages A-D. However, pages B and D are actually part of pages A and C [0069-0070]. This is done to create a symmetry that allows the reduction of the number of cases that need to be considered for packetization [0068]. McGuinness describes interlacing the luminance Y and both chrominance Cr and Cb so that all of the components can be retrieved in one word, reducing latency during rasterization without increasing the time needed to retrieve pixels for decoding because all of the components for one tile can still be retrieved in one burst (Col. 10, lines 26-30). Storing the chrominance components so interlaced enables the FIFO that stores the chrominance to have the same structure as the FIFO storing the luminance (Col. 10, lines 8-9), and therefore creates symmetry. Therefore, McGuinness discloses the step of placing a virtual memory page boundary across the chrominance chunk, the virtual memory page boundary being associated with the packetization scheme. This would be obvious for the same reasons given in the rejection for Claim 10.

26. With regard to Claim 18, Rege does not specifically teach that the plurality of data packets comprise 16 words. However, McGuinness describes that the plurality of data packets comprise 16 words (Col. 9, lines 7-11).

It would have been obvious to one of ordinary skill in the art to modify the device of Rege so that the plurality of data packets comprise 16 words as suggested by

McGuinness because McGuinness suggests that this is a common size for a data packet (Col. 9, lines 7-11).

27. With regard to Claim 20, Claim 20 is similar in scope to Claim 4, and therefore is rejected under the same rationale.

28. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A) and McGuinness (US006104416A) in view of Sorin (US006631164B1).

29. With regard to Claim 5, Rege and McGuinness are relied upon for the teachings as discussed above relative to Claim 4.

However, Rege and McGuinness do not teach that the step of determining the location of the read data further comprises receiving at least a set of motion vectors pointing to the reference pixel chunk. However, Sorin discloses that the step of determining the location of the read data further comprises receiving at least a set of motion vectors pointing to the reference pixel chunk (*access to a predicted block, on the basis of a motion vector, predicted blocks to be read from the memory and defined by the motion vectors, motion vector is accurate to within half a pixel*, Col. 6, lines 31-45).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Rege and McGuinness's MPEG device (Col. 4, lines 60-62) so that the step of determining the location of the read data further comprises receiving at least a set of motion vectors pointing to the reference pixel chunk

as suggested by Sorin because Sorin suggests that motion vectors are needed in order to perform motion estimation to produce high quality MPEG digital video data of an image (Col. 1, lines 30-39, 66-67; Col. 2, lines 1-2).

30. With regard to Claim 6, Rege and McGuinness do not teach the step of determining a first set of components associated with the reference pixel chunk based on the at least a set of motion vectors. However, Sorin discloses the step of determining a first set of components associated with the reference pixel chunk based on the at least a set of motion vectors (Col. 6, lines 31-45). This would be obvious for the same reasons given in the rejection for Claim 5.

31. With regard to Claim 7, Rege and McGuinness do not teach that the step of selecting a packetization scheme further comprises combining a part of the luminance chunk and a part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages. However, Sorin discloses accessing blocks by combining them in a certain manner (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39). Therefore, Sorin describes that the step of selecting a combining scheme further comprises combining a part of the luminance chunk and a part of the chrominance chunk into one of the plurality of macroblocks to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Rege and McGuinness's MPEG device (Col. 4, lines 60-62) so that the step of selecting a packetization scheme further comprises combining a part of the luminance chunk and a part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages as suggested by suggests that this reduces the number of pages changes needed to access the MPEG digital video data of an image (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39), which enables the data to be accessed faster (Col. 3, lines 28-37).

32. With regard to Claim 8, Rege and McGuinness do not teach that the step of selecting a packetization scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages. However, Sorin discloses accessing blocks by combining them in a certain manner (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39). Therefore, Sorin describes that the step of selecting a combining scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of macroblocks to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Rege and McGuinness's MPEG device

(Col. 4, lines 60-62) so that the step of selecting a packetization scheme further comprises combining a first part of the luminance chunk and a second part of the luminance chunk into one of the plurality of data packets to be sent from the memory when the luminance chunk overlaps more than one of the plurality of memory pages as suggested by Sorin. Sorin suggests that typically, motion estimation calculations are performed on the luminance values alone, for MPEG digital video data of an image (Col. 1, lines 46-61). This also reduces the number of pages changes needed to access the MPEG digital video data of an image (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39), which enables the data to be accessed faster (Col. 3, lines 28-37).

33. With regard to Claim 9, Rege and McGuinness do not teach that the step of selecting a packetization scheme further comprises combining a first part of the chrominance chunk and a second part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the chrominance chunk overlaps more than one of the plurality of memory pages. However, Sorin discloses accessing blocks by combining them in a certain manner (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39). However, Sorin discloses the step of selecting a combining scheme further comprises combining a first part of the chrominance chunk and a second part of the chrominance chunk into one of the plurality of macroblocks to be sent from the memory when the chrominance chunk overlaps more than one of the plurality of memory pages (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Rege and McGuinness's MPEG device

(Col. 4, lines 60-62) so that the step of selecting a packetization scheme further comprises combining a first part of the chrominance chunk and a second part of the chrominance chunk into one of the plurality of data packets to be sent from the memory when the chrominance chunk overlaps more than one of the plurality of memory pages as suggested by Sorin because Sorin suggests the advantage of being able to combining the blocks for greater transfer efficiency based on whether luminance data alone is needed, chrominance data alone is needed, or both luminance data and chrominance data are needed (Col. 6, lines 36-39). This also reduces the number of pages changes needed to access the MPEG digital video data of an image (Col. 4, line 64-Col. 5, line 5; Col. 6, lines 36-39), which enables the data to be accessed faster (Col. 3, lines 28-37).

34. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A) in view of Levy (US005170251A).

Rege is relied upon for the teachings as discussed above relative to Claim 1. Rege discloses packet data is stored in an array of pages 305, which are 512 bytes large. Packets smaller than 512 bytes are stored in one page 305, packets between 512 and 1024 bytes are stored in two pages 305, etc. (Col. 6, lines 12-22). Each of the pages has a plurality of words (Col. 6, lines 60-65). Therefore, Rege describes that the packetization scheme selected maps packet data (a first set of components) to selected ones of the array of pages 305 containing a plurality of words (a second set of components). Claim 13 recites that the first set of components comprises the data and the second set of components comprises the selected ones of the plurality of words. Therefore, Rege

discloses that the packetization scheme selected maps a first set of components (packet data) to a second set of components (selected ones of the plurality of words).

However, Rege does not teach selecting the packetization scheme by a table lookup. However, Levy describes selecting the packetization scheme by a table lookup (Col. 2, lines 20-30).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Rege to include selecting the packetization scheme by a table lookup as suggested by Levy. The speed gained by using a lookup table can be significant, since retrieving a value from memory is often faster than undergoing an expensive computation, and this is well-known in the art.

35. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rege (US005390299A) and Levy (US005170251A) in view of McGuinness (US006104416A).

Rege and Levy are relied upon for the teachings as discussed above relative to Claim 12.

However, Rege and Levy do not teach that the first set of components comprises the read data corresponding to the luminance chunk and the chrominance chunk, and the second set of components comprises the selected ones of the plurality of words. However, McGuinness discloses that the first set of components comprises the read data corresponding to the luminance chunk and the chrominance chunk, and the second set of components comprises the selected ones of the plurality of words (Col. 9, lines 55-59; Col. 10, lines 4-7).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Rege and Levy so that the first set of components comprises the read data corresponding to the luminance chunk and the chrominance chunk, and the second set of components comprises the selected ones of the plurality of words as suggested by McGuinness because McGuinness suggests that this allows for the interlacing of the chrominance components in such a manner as to allow the chrominance components to be retrieved in one word, reducing latency during rasterization, and because all of the chrominance for one tile can still be retrieved in one burst the time to retrieve the chrominance for decoding is not increased (Col. 9, lines 60-65). Storing the chrominance components so interlaced enables the FIFO that stores to chrominance to have the same structure as the FIFO storing the luminance, so that different structured FIFOs are not required (Col. 10, lines 8-17). This increases the efficiency of retrieving encoded bitstreams for video (Col. 2, lines 8-18). It would have been obvious to modify Rege's method of selecting a packetization scheme so that it is used for reading an encoded bitstream for video for the same reasons given in the rejection for Claim 4.

36. Claims 21-23 and 28-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Artieri (US005579052A) in view of Rege (US005390299A).

37. With regard to Claim 21, Artieri discloses a method for reassembling reference pixel data from a plurality of data packets into a luminance chunk and a chrominance chunk (Col. 18, lines 21-37; Col. 3, lines 34-51), comprising the steps of receiving the

plurality of data packets, each data packet comprising a portion of a reference pixel chunk including the luminance chunk and the chrominance chunk; determining a scheme used to output the luminance and chrominance chunks in the plurality of data packets based upon the locations in memory of the data; and unpacking the plurality of data packets into a reassembled luminance chunk and a reassembled chrominance chunk based on the scheme (Col. 1, lines 30-45; Col. 3, lines 34-51). Artieri discloses determining the position in the picture memory from which packets of data must be transferred. The instruction processor includes an address register containing the address at which a read operation is carried out. After determining the position, the content of the address register is modified. This modification may consist in an incrementation (which amount to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks) (Col. 16, lines 33-47). Therefore, based on the locations of the read data, the packets can be combined by reading data at successive addresses, or the packets can be combined by a more complex calculation, such as a recursive calculation to extract a picture line from a sequence of macro-blocks. Therefore, Artieri discloses selecting a scheme based upon the location in the memory and then combining the data into packets according to that scheme.

However, Artieri does not teach determining a packetization scheme used to **packetize** the luminance and chrominance chunks into the plurality of data packets based upon the locations in memory of the data; and unpacking based on the packetization scheme. However, Rege discloses determining a packetization scheme used to packetize the data into the plurality of data packets based upon the locations in memory of the data;

and unpacking based on the packetization scheme (Col. 6, lines 60-68; Col. 7, lines 1-12, 36-48).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Artieri to include determining a packetization scheme used to packetize the luminance and chrominance chunks into the plurality of data packets based upon the locations in memory of the data; and unpacking based on the packetization scheme as suggested by Rege because Rege suggests that if more that one page of data needs to be transferred, it can be transferred in one packet, therefore increasing the transferring efficiency (Col. 6, lines 18-22).

38. With regard to Claim 22, Artieri discloses the steps of forming prediction blocks by arranging the plurality of data packets unpacked with any information related to motion vectors (Col. 1, lines 36-45; Col. 3, lines 34-50), and combining blocks with associated macroblocks to form a reconstructed macroblock (*macro-block is combined with two predictor macro-blocks, these two pictures are respectively former and subsequent pictures, with respect to the currently reconstructed picture*, Col. 1, line 64-Col. 2, line 3).

39. With regard to Claim 23, Artieri discloses the step of writing the reconstructed macroblock to a memory (*store the currently reconstructed picture*, Col. 7, lines 47-50) having a plurality of memory pages; selecting a packetization scheme based on a location of read data and on fitting the read data into the plurality of data packets; and assembling

at least one read command for fetching the read data from the memory in accordance with the packetization scheme selected (Col. 16, lines 32-47).

However, Artieri does not teach that at least one data packet contains data from more than one of the plurality of memory pages. However, Rege discloses that at least one data packet contains data from more than one of the plurality of memory pages (Col. 6, lines 18-22). This would be obvious for the same reasons given in the rejection for Claim 21.

40. With regard to Claim 28, Artieri discloses a system for decoding pictures in a compressed video bit stream (*picture decompression system*, Col. 3, lines 6-8; *MPEG decoder*, Col. 6, lines 33-34), comprising a memory (15, Figure 3; Col. 6, lines 37-41) having a plurality of memory pages (Col. 18, lines 21-30) storing reference pixel data (Col. 7, lines 52-67); an address generator (24) coupled to the memory for generating memory commands for fetching the reference pixel data from the memory; means for packing the fetched reference pixel data into a plurality of data packets according to the specifications of the memory commands (*determine the position in the picture memory from which packets of data must be transferred, instruction processor includes an address register containing the address at which a transfer operation is carried out, instructions to adequately modify the content of the address register, this adequate modification may consist in an incrementation (which amount to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks),* Col. 16, lines 32-47; *memory controller 24 includes instruction processing unit*

50, Col. 13, lines 18-25); a reference data assembly module (FIFOs) coupled to the address generator for receiving from the memory the plurality of data packets (*exchanges on the MBUS are controlled by a memory controller 24 that serves to carry out, transfer operations between these FIFOs and the picture memory*, Col. 6, lines 45-48); and means for unpacking the plurality of data packets and resassembling the fetched reference pixel data into a reassembled video bit stream (*macro-block is reconstructed by using a predictor macro-block fetched in a previously decoded picture*, Col. 1, lines 36-45; *receives the compressed data from the memory bus and extracts the packets therefrom*, Col. 3, lines 34-50). Artieri discloses determining the position in the picture memory from which packets of data must be transferred. The instruction processor includes an address register containing the address at which a read operation is carried out. After determining the position, the content of the address register is modified. This modification may consist in an incrementation (which amount to write or to read data at successive addresses in the picture memory) or in a more complex calculation (for example a recursive calculation to extract a picture line from a sequence of macro-blocks) (Col. 16, lines 33-47). Therefore, based on the locations of the read data, the packets can be combined by reading data at successive addresses, or the packets can be combined by a more complex calculation, such as a recursive calculation to extract a picture line from a sequence of macro-blocks. Therefore, Artieri discloses packing the fetched reference pixel data into a plurality of data packets according to the specifications of the memory commands.

However, Artieri does not teach that at least one data packet contains data from more than one of the plurality of memory pages. However, Rege discloses that at least

one data packet contains data from more than one of the plurality of memory pages (Col. 6, lines 18-22). This would be obvious for the same reasons given in the rejection for Claim 21.

41. With regard to Claim 29, Artieri discloses that the reference pixel data comprises a luminance chunk and a chrominance chunk (Col. 1, lines 30-45).

42. With regard to Claim 30, Artieri discloses that the memory commands comprises specification for combining selected portions of the reference pixel data from a selected one or more of the plurality of memory pages into at least one of the plurality of data packets (Col. 16, lines 32-47).

43. With regard to Claim 31, Artieri discloses that the reference data assembly module (FIFO) unpacks the plurality of data packets to transform the reference pixel data into a reassembled luminance chunk and a reassembled chrominance chunk (*the luminance block is stored in a first page and the chrominance block is stored in another page*, Col. 18, lines 31-37; *memory controller 24 then transfers the compressed data from memory 15 to the FIFO 21, in the order they were written*, Col. 10, lines 16-18).

44. With regard to Claim 32, Artieri discloses that the reference data assembly module comprises a plurality of data buffers, each data buffer being configured to receive one of the plurality of data packets (*the size of the FIFOs is two packets of data, one packet of data corresponding to a macro-block fraction*, Col. 9, lines 45-48).

45. With regard to Claim 33, Artieri discloses that the reference data assembly module comprises an additional module (14, Figure 3) for reassembling the reference pixel data based on a set of motion vectors (*once it has received the macro-block type and the vectors, the filter 14 is ready to receive a predictor macro-block*, Col. 10, lines 32-34; *filter 14 includes two FIFOs; one FIFO is intended to receive forward macro-block; the other FIFO is intended to receive backward macro-blocks*, Col. 10, lines 52-65; *macro-block is reconstructed by using a predictor macro-block, movement compensation vector that defines the position of the predictor macro-block,* Col. 1, lines 39-45) and packetization scheme used to form the plurality of data packets (*FIFO of filter 14*, Col. 11, lines 26-34; *size of the FIFOs is two packets of data*, Col. 9, lines 45-52).

However, Artieri does not teach a table lookup used to form the plurality of data packets. However, Levy describes a table lookup used to form the plurality of data packets (Col. 2, lines 20-30), as discussed in the rejection for Claim 12.

46. With regard to Claim 34, Artieri discloses that the reference data assembly module comprises a plurality of data buffers for buffering a reassembled luminance chunk and a reassembled chrominance chunk (Col. 18, lines 31-37; Col. 10, lines 16-18).

47. With regard to Claim 35, Artieri discloses a variable length decoding module (10, Figure 3) configured to extract a set of motion vectors corresponding to a macroblock in the compressed video bit stream (*movement compensation vectors, these decoding parameters are decoded by the VLD circuit itself to decode the vectors and data of the*

macro-blocks, Col. 7, lines 10-15; *MPEG decoder, couples the compressed data input bus to the input of the variable length decoder (VLD) 10*, Col. 6, lines 33-39).

48. With regard to Claim 36, Artieri discloses that the variable length decoding module (10, Figure 3) sends the extracted set of motion vectors to the address generator (24) (Col. 7, lines 10-15).

49. With regard to Claim 37, Artieri discloses a memory interface unit (instruction register) coupled to the memory (*instruction register is coupled to the output of ROM 54, an instruction is executed substantially as soon as it is loaded in the instruction processor 50*, Col. 13, lines 59-64).

50. With regard to Claim 38, Artieri discloses that the memory interface unit further comprises a memory queue for storing the generated memory commands from the address generator (Col. 13, lines 59-64).

51. With regard to Claim 39, Artieri discloses that at least one of the plurality of data packets includes the reference pixel data from at least two of the plurality of memory pages (Col. 18, lines 31-37) based on the generated memory commands in the memory queue (Col. 16, lines 32-47; Col. 13, lines 59-64).

52. With regard to Claim 40, Artieri discloses that the memory interface unit (24, Figure 5; Col. 13, lines 18-25) further comprises a sequencer for forwarding the

generated memory commands to the memory to obtain the reference pixel data based on specifications (*the beginning of a transfer program of a packet of data includes an instruction that writes in this address register the content of the data pointer,* Col. 16, lines 32-47).

53. With regard to Claim 41, Artieri discloses that the memory interface unit (24) further comprises a packet assembly unit (FIFO) for assembling the plurality of data packets of the reference pixel data obtained from the memory (Col. 6, lines 45-51; Col. 9, lines 45-52).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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